What is claimed is:

1. A motherboard in a computing system, wherein said motherboard comprises:

a circuit board including a main voltage plane segment and a separate voltage plane segment;

a microprocessor;

a port connector including a connection-sensing terminal;

switching means for selectively connecting said main voltage plane segment to said separate voltage plane segment, wherein said switching means connects said main voltage plane segment to said separate voltage plane segment in response to a determination that said connection-sensing terminal is externally grounded, and wherein switching means disconnects said main voltage plane segment from said separate voltage plane segment in response to a determination that said connection-sensing terminal is electrically floating; and

a device interface circuit conditioning signals transmitted between said microprocessor and said port connector, wherein said device interface circuit draws electrical power from said separate voltage plane segment.

2. The motherboard of claim 1, wherein

said switching means includes a biasing resistor and a switching device,

said switching device has a control terminal connected to said connection-sensing terminal and connected to a biasing voltage through said biasing resistor, an input terminal connected to said main voltage plane segment, and an output terminal connected to said separate voltage plane segment,

said input terminal is connected to said output terminal in response to an application of electrical ground to said control terminal, and

said input terminal is disconnected from said output terminal in response to an application of said biasing voltage to said control terminal.

3. The motherboard of claim 2, wherein

said switching device includes a field effect transistor,

said control terminal includes a gate of said field effect transistor,

said input terminal includes a source of said field effect transistor, and

said output terminal includes a sink of said field effect transistor.

4. The motherboard of claim 2, wherein said biasing resistor is connected to said biasing voltage at said main voltage plane.

5. The motherboard of claim 1, wherein

said motherboard additionally comprises non-volatile storage,

said switching means includes a biasing resistor, first and second registers, a switching device, and a switching routine stored within said non-volatile storage for execution within said microprocessor,

said first register includes an input terminal connected to said connection-sensing terminal and connected to a biasing voltage through said biasing resistor,

said first register is driven to a first state by an application of electrical ground to said input terminal and to a second state by an application of said biasing voltage to said input terminal,

said switching routine executing within said microprocessor drives said second register into a third state in response to a determination that said first register is in said first state,

said switching routine executing within said microprocessor drives said second register into a fourth state in response to a determination that said first register is in said second state,

said switching device has a control terminal connected to an output of said second register, an input terminal connected to said main voltage plane segment, and an output terminal connected to said separate voltage plane segment,

said input terminal is connected to said output terminal in response to a signal applied to said control terminal from said output of said second register when said second register is in said third state, and

said input terminal is disconnected from said output terminal in response to a signal applied to said control terminal from said output of said second register when said second register is in said fourth state.

6. The motherboard of claim 5, wherein

said switching device includes a field effect transistor,

said control terminal includes a gate of said field effect transistor,

said input terminal includes a source of said field effect transistor, and

said output terminal includes a sink of said field effect transistor.

7. The motherboard of claim 5, wherein said biasing resistor is connected to said biasing voltage at said main voltage plane.

8. The motherboard of claim 5, wherein said switching routine executing within said microprocessor periodically examines a state of said first register in response to clock pulses.

9. The motherboard of claim 5, wherein said switching routine executing within said microprocessor additionally causes a device driver routine used to condition signals transferred through said port connector to be loaded in response to a determination that said first register is in said first state and that said second register is in said third state.

10. The motherboard of claim 5, wherein said switching routine executing within said microprocessor additionally causes a device driver routine used to condition signals transferred through said port connector to be unloaded in response to a

determination that said first register is in said second state and that said second register is in said fourth state.

11. The motherboard of claim 5, wherein

said non-volatile storage additionally holds a system pausing subroutine for execution within said microprocessor in response to an attempt to write or read data through said port connector,

said system pausing subroutine causes a message to be displayed indicating a cable is disconnected and provides a graphical user interface for selecting a retry after said cable is connected, in response to a determination that said second register is in said fourth state, and

said system pausing subroutine causes said attempt to write or read data through said port connector to be retried in response to receiving a selection of said retry from said graphical user interface.

12. A motherboard in a computing system, wherein said motherboard comprises:

a circuit board including a main voltage plane segment;

a microprocessor; and

a plurality of connection subsystems, wherein each connection system within said plurality of connection subsystems includes:

a separate voltage plane segment within said circuit board;

a port connector including a connection-sensing terminal;

switching means for selectively connecting said main voltage plane segment to said separate voltage plane segment, wherein said switching means connects said main voltage plane segment to said separate voltage plane segment in response to a determination that said connection-sensing terminal is externally grounded, and wherein switching means disconnects said main voltage plane segment from said separate voltage plane segment in response to a determination that said connection-sensing terminal is electrically floating; and

a device interface circuit conditioning signals transmitted between said microprocessor and said port connector, wherein said device interface circuit draws electrical power from said separate voltage plane segment.

13. The motherboard of claim 12, wherein, within each said connection subsystem,

said switching means includes a biasing resistor and a switching device,

said switching device has a control terminal connected to said connection-sensing terminal and connected to a biasing voltage through said biasing resistor, an input terminal connected to said main voltage plane segment, and an output terminal connected to said separate voltage plane segment,

said input terminal is connected to said output terminal in response to an application of electrical ground to said control terminal, and

said input terminal is disconnected from said output terminal in response to an application of said biasing voltage to said control terminal.

14. The motherboard of claim 12,

wherein said motherboard additionally comprises first and second registers and non-volatile storage storing a switching routine for execution within said microprocessor,

wherein, within each said connection subsystem,

said switching means includes a biasing resistor, bit positions within said first and second registers, and a switching device,

said bit position within said first register includes an input terminal connected to said connection-sensing terminal and connected to a biasing voltage through said biasing resistor, and

said bit position within said first register is driven to a first state by an application of electrical ground to said input terminal and to a second state by an application of said biasing voltage to said input terminal,

said switching routine executing within said microprocessor drives said bit position within said second register into a third state in response to a determination that bit position of said first register is in said first state,

said switching routine executing within said microprocessor drives said second register into a fourth state in response to a determination that said bit position in said first register is in said second state, and

wherein, within each said connection subsystem,

said switching device has a control terminal connected to an output of said second register, an input terminal connected to said main voltage plane segment, and an output terminal connected to said separate voltage plane segment,

said input terminal is connected to said output terminal in response to a signal applied to said control terminal from said output of said second register when said second register is in said third state, and

said input termi1nal is disconnected from said output terminal in response to a signal applied to said control terminal from said output of said second register when said second register is in said fourth state.

15. The motherboard of claim 14, wherein for each said connection subsystem, said switching routine executing within said microprocessor additionally causes a device driver routine used to condition signals transferred through said port connector to be loaded in response to a determination that said first register is in said first state and that said second register is in said third state.

16. The motherboard of claim 14, wherein for each said connection subsystem, said switching routine executing within said microprocessor additionally causes a device driver routine used to condition signals transferred through said port connector to be unloaded in response to a determination that

said first register is in said second state and that said second register is in said fourth state.

17. The motherboard of claim 14, wherein

said non-volatile storage additionally holds a system pausing subroutine for execution within said microprocessor in response to an attempt to write or read data through a port connector within a connection subsystem in said plurality of connection subsystems,

said system pausing subroutine causes a message to be displayed indicating an external cable to said port connector is disconnected and provides a graphical user interface for selecting a retry after said external cable is connected, in response to a determination that said second register within said connection subsystem is in said fourth state, and

said system pausing subroutine causes said attempt to write or read data through said port connector to be retried in response to receiving a selection of said retry from said graphical user interface.

18. A system configuration method for switching electrical power to each device interface circuit within a plurality of device interface circuits, wherein each said device interface circuit conditions signals transmitted between a microprocessor and a port connector electrically connected to said device interface circuit, and wherein said system configuration method comprises:

for each said device interface circuit, setting a bit position associated with said device interface circuit in a first register to a first state in response to electrically grounding a connection-sensing terminal within said port connector connected to said device interface circuit and to a second state in response to electrically floating said connection-sensing terminal; and

for each device interface circuit within said plurality of device interface circuits, performing a port configuration method including:

reading said bit position associated with said device interface circuit within said first register;

reading a bit position associated with said device interface circuit within a second register;

setting a bit position associated with said device interface circuit in said second register to a third state in response to determining that said bit position associated with said device interface circuit in said first register is in said first state and that said bit position associated with said device interface circuit in said second register is in a fourth state;

setting said bit position associated with said device interface circuit in said second register to said fourth state in response to determining that said bit position associated with said device interface circuit in said first register is in said second state and that said bit position associated with said device circuit in said second register is in said third state;

turning a switching device on to conduct electrical power to said device interface circuit in response to setting said bit position associated with said device interface circuit in said second register to said third state; and

turning said switching device off in response to setting said bit p position associated with said device interface circuit in said second register to said fourth state.

19. The method of claim 18, wherein said port configuration method additionally includes:

loading a device driver routine used during operation of said device interface circuit in response to determining that said bit position associated with said device interface circuit in said first register is in said first state and that said bit position associated with said device interface circuit in said second register is in said fourth state; and

unloading a device driver routine used during operation of said device interface circuit in response to determining that said bit position associated with said device interface circuit in said first register is in said second state and that said bit position associated with said device circuit in said second register is in said third state.

20. The system configuration method of claim 18, additionally comprising:

following a first step attempting to write data through a device interface circuit in said plurality of device interface circuits, performing a system pausing method comprising:

reading a bit position set to indicate whether electrical power is supplied to said device interface circuit;

in response to determining that electrical power is not supplied to said device interface circuit, displaying a message indicating a cable is not attached to said port connector electrically connected to said device interface circuit and providing a graphical user interface allowing a user selection to continue after connecting a cable to said port connector; and

in response to receiving an input from said graphical user interface, again attempting to write data through said device interface circuit; and

following a first step attempting to read data through a device interface circuit in said plurality of device interface circuits, performing a system pausing method comprising:

reading a bit position set to indicate whether electrical power is supplied to said device interface circuit;

in response to determining that electrical power is not supplied to said device interface circuit, displaying a message indicating a cable is not attached to said port connector electrically connected to said device interface circuit and providing a graphical user interface allowing a user selection to continue after connecting a cable to said port connector; and

in response to receiving an input from said graphical user interface, again attempting to read data through said device interface circuit.